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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,657	03/11/2004	Stephen M. Prather	5298-13101 CD02212	6316

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,657	PRATHER ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-16,18 and 19* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6, 8-16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (U. S. PAT. 4,906,871).

In claim 1, Iida teaches all claimed features in Figs 3 and 5-7, a circuit, comprising: a differential amplifier (13); a capacitor (19) coupled to an output (a terminal coupled to a node at R3 opposite to Vcc) of the differential amplifier; an inverter (20) coupled to the capacitor; and a biasing circuit (Q7 or Q8) comprises a transmission gate consisting of a p-channel transistor (Q8) coupled in parallel with an n-channel transistor (Q7) between the capacitor and the inverter (as shown in Figs. 5-7); with the exception of teaching wherein a gate terminal of the p-channel transistor is coupled to a power down voltage at a power supply voltage and a gate terminal of the n-channel transistor is coupled to a ground voltage during power down of the circuit. However, it is so obvious to one ordinary skill in the art to rearrange the connections of the p-channel and the n-channel of Iida in the opposite manner, during power down the circuit; since there is no additional circuitry involved and it only involves reversing logic levels at the gates of the p-channel and n-channel transistors. Furthermore, it would have been obvious to one ordinary skill in the art at the time of the invention was made to rearrange the logic

levels at the gates of the p-channel and n-channel transistors of lida circuit, during power down the circuit; since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to arrange the logic levels at the gates of the p-channel and n-channel transistors of lida circuit, during power down the circuit, in order to present another version of lida circuit.

In claim 2, lida further teaches the circuit as recited in claim 1, wherein the inverter (20) comprises a p-channel transistor (Q5) coupled in series with an n-channel transistor (Q6).

In claim 3, lida further teaches the circuit as recited in claim 1, the circuit as recited in claim 1, wherein the capacitor (19) comprises a pair of conductive terminals (terminals of 19) separated by a dielectric (inherent), and wherein a first terminal of the pair of terminals is coupled to the output (the terminal coupled to the node at R3 opposite to Vcc) of the differential amplifier and a second terminal of the pair of terminals is coupled to the inverter (20).

In claim 4, lida further teaches the circuit as recited in claim 1, wherein the inverter (20) comprises a terminal (as shown) coupled to the capacitor (19).

In claim 6, lida further teaches in Fig. 7, the circuit as recited in claim 1, wherein a gate terminal of the p-channel transistor (Q8) is coupled to the power down voltage (0V) and a gate terminal of the n-channel transistor (Q7) is coupled to the power supply voltage (Vcc or logic 1) during operation of the circuit.

In claims 8 and 9, Iida further teaches in Fig. 8 the circuit as recited in claim 1, the circuit as recited in claim 1, wherein the biasing circuit comprises a second inverter (22); and wherein the second inverter comprises both an input and an output coupled to the capacitor (via R6).

In claim 10, it is believed that Iida further teaches in Fig. 8 wherein the inverter (20) comprises a first p-channel transistor (Q5) and an first n-channel transistor (Q6) having substantially the same gate length but having a first p-channel gate width at a first ratio relative to first n-channel gate width, and wherein the second inverter (22) comprises second p-channel transistor (Q9) and a second n-channel transistor (Q10) having substantially the same gate length but having a second p-channel gate width at a second ratio relative to a second n-channel gate width, and wherein the first ratio is approximately equal to the second ratio. Further more, it would have been obvious to one ordinary skill in the art to modify the gate length or the gate width of transistors is a matter of design choice, since such modification would have been involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to modify the sizes of transistors within the inverters is a matter of design choice.

In claim 11, Iida teaches all claimed features in Figs. 1, 3 and 5-7, a receiver, comprising: an inverter (20); a differential amplifier (13) adapted to receive a differential input signal (base terminals for T1 and T2) forwarded to the receiver from a

transmission medium (differential lines connected to 18); a biasing circuit (Q7, Q8 in Fig. 7) coupled to an input of the inverter (20) to bias a voltage on the inverter to a trip point of the inverter; and capacitor (19) coupled between the inverter and respective output (one end of resistor R3) of the differential amplifier (13) to place upon the inverter change in voltage centered around the trip point, wherein the change in voltage correspond to change in amplitude of the differential input signal; with the exception of teaching a second inverter and a second bias circuit coupling to the other output of the differential amplifier (13), Iida just shows one output line. However, it is obvious to one ordinary skill in the art to set up or duplicate another inverter and bias circuit, which is identical to what already shown output line in Fig. 3 of Iida, attaching to the output of the differential amplifier (13) at the end of R4, in order to obtain differential output signals.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to duplicate another inverter and bias circuit (mirror image), which is identical to the already shown output line of Iida in order to provide a differential CMOS level shifter circuit.

Claim 12, Iida further teaches the receiver as recited in claim 11, wherein each of the pair of inverters (only one of the inverter shown, 20) is a complementary metal oxide semiconductor (CMOS) inverter.

In claim 13, Iida further teaches the receiver as recited in claim 11, wherein the biasing circuit comprises a transmission gate (Q7 or Q8) coupled between the input and output of each of the pair of inverters to maintain a direct current (DC) voltage bias on

the input of each of the pair of inverters approximately at the trip point (V1) of the inverters.

In claim 14, Iida further teaches the receiver as recited in claim 11, wherein the transmission gate comprises a p-channel transistor (Q8) coupled in parallel with an n-channel transistor (Q7), wherein, during operation, a gate terminal of the p-channel transistor is coupled to a power down voltage at a ground supply voltage (logic 0 turns ON p-channel transistor) and a gate terminal of the n-channel is coupled to a power supply voltage (logic 1 turns on n-channel transistor), and wherein during non-operation (as discussed in claim 1), the gate terminal of the p-channel transistor is coupled to the power supply voltage (logic 1) and a gate terminal of the n-channel is coupled to the ground supply voltage (logic 0).

In claims 15 and 16, Iida further teaches the receiver as recited in claim 11, wherein the biasing circuit comprises a second inverter (22) having an input coupled to an output of the inverter and also having an output coupled to an input of the inverter (as shown in Fig. 8); and wherein the ratio of gate widths p-channel and n-channel transistors of the first inverter and the second inverter are substantially equal.

Method claims 18-19 correspond to detailed circuitry already discussed similarly with regard to claims 11-16.

3. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Argument

4. Applicant's arguments filed 1/27/2006 have been fully considered but they are not persuasive. In claim 1, as discussed above, it is so obvious to one ordinary skill in the art to rearrange the connections of the p-channel and the n-channel of Iida in the opposite manner, during power down the circuit; since there is no additional circuitry involved and it only involves reversing logic levels at the gates of the p-channel and n-channel transistors. And, in claim 11, it is also obvious to one ordinary skill in the art to set up or duplicate another inverter and bias circuit, which is identical to what already shown output line in Fig. 3 of Iida, attaching to the output of the differential amplifier (13) at the end of R4, in order to obtain differential output signals.

5. The rejection of claims 1-4, 6, 8-16, 18 and 19 is maintained.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER